



## 14-bit 250MSPS four-channel Analog-to-Digital Converter (ADC)

### 1 Main features:

- ◆ Converted bits: 14 bits
- ◆ Clock frequency: 250 MSPS
- ◆ Supply voltage: 3.3/1.9/1.8V
- ◆ Power consumption: 400 mW/CH
- ◆ Data interface: LVDS interface
- ◆ SFDR : 90dBc@170MHzinput
- ◆ SNR : 69dBFS@170MHzinput
- ◆ Optional in-film jitter
- ◆ ADC internal reference voltage source
- ◆ Encapsulation : BGA144

### 2. Typical applications

- ◆ Wireless communication system
- ◆ Intelligent antenna system
- ◆ Software radio
- ◆ Broadband data application
- ◆ Medical ultrasound equipment
- ◆ Radar and aviation systems

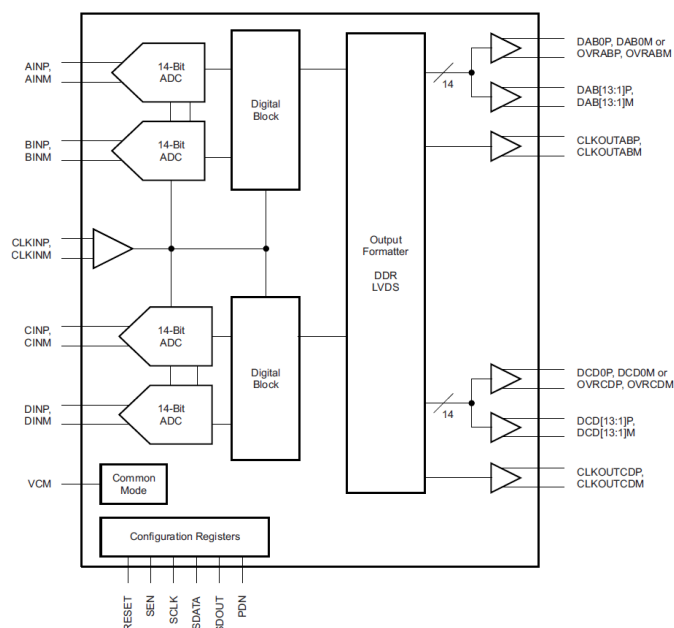
### 3 Product Description

The chip is a 14-bit, 250 MSPS single-channel ADC designed for communication applications requiring high performance, low cost, and small size. The ADC core uses a multi-level, differential pipeline architecture and integrates output error correction logic. The front-end wideband differential sampling and holding circuit allows users to flexibly select various input ranges.

### 5 Compared with similar foreign products

	precision	Clock frequency	Data port	CH power consumption	SNR	SFDR	Encapsulation form
ADS4449 (TI)	14Bit	250MHz	LVDS	373mW@250MSPS	69dBFS@170MHz	86dBc@170 MHz	BGA144
AD9643 (ADI)	14Bit	250MSPS	LVDS	392mW@250MSPS	70.6dBFS@185MHz	85dBc@185 MHz	QFN48
HL4449	14Bit	250MHz	LVDS	400mW@125MSPS	69dBFS@170MHz	90dBc@170 MHz	BGA144

The reference voltage circuit is integrated in the chip. The chip has a clock duty ratio regulator, which can compensate the fluctuation of ADC clock duty ratio and ensure the output performance of the converter. The chip output is LVDS signal. The chip has a power saving mode to reduce power consumption. The chip uses a four-wire SPI interface to realize various configurations. The chip adopts BGA144 package and is compatible with foreign products ADS4449 pin, which can be replaced. The internal structure block diagram of the chip is as follows:



### 4 Product Highlights

- ◆ Optional on-chip jitter option improves small-signal SFDR performance.
- ◆ Proprietary differential inputs maintain excellent SNR at 300 MHz input frequencies.
- ◆ Standard serial port configuration: output data format, clock DCS enable, power saving mode, test mode, reference voltage value, etc.